NCP6868

Product Preview

2.5 A-DC Boost Regulator with By-Pass Function

The NCP6868 is a synchronous boost converter. It is designed primarily to boost new generation Low-Voltage Li-Ion Batteries (silicon anode-like) embedded into cell and smart phones. The objective is to guarantee a minimum output voltage even in the case for which the battery voltage is below the minimum voltage required by the system. The device features a By-pass mode coupled with a Boost mode. It is capable to drive a load up to 2.5 A continuous, operates at a switching frequency of 2.5 MHz. An I^2C serial control can also be enabled for configuring the output voltage and peak current limit. The NCP6868 is available in a space saving, low profile 1.8×1.8 mm CSP-16 package.

Features

- 2.35 V to 5.5 V Input Voltage
- Fixed or Programmable V_{OUT}: from 2.85 V up to 5.3 V
- Bypass Operation when V_{IN} Above or Close to V_{OUT}
- Few External Components & 0.47 μH Inductor
- High Efficiency Up to 95%
- Output Current Up to 2.5 A Continuous (V_{IN} = 2.6 V, V_{OUT} = 3.5 V) and up to 4 A Peak Current
- Inductor Peak Current up to 9.0 A
- Forced Bypass Option through $\overline{BP}$ Pin
- Low Quiescent Current
- Voltage Control Pin (VSEL) to Precisely Adjust V_{OUT}
- I^2C Serial Control as a Software-Mode Option to Program Output Voltage and Peak Current Limit
- Soft-Start Function (SS) to Limit Inrush Current
- Current Limitation to Protect Against Short Circuit
- Thermal Limit Protection
- Small 1.8×1.8 mm / 0.4 mm Pitch CSP Package

Typical Applications

- Boost Converters for New Generation Low-Voltage Li-Ion Batteries
- USB OTG (On-The-Go)
- 3G/4G – LTE RF PA
- Cell Phones, Smart Phones, Phablets, Tablets & Webtablets

This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice.

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WLCSP16
CASE 567JU

MARKING DIAGRAM

6868= Specific Device Code
xxxx = Device Version
A = Assembly Location
L = Wafer Lot
YY = Year
WW = Work Week
▪ = Pb−Free Package

ORDERING INFORMATION

See detailed ordering and shipping information on page 27 of this data sheet.

TYPICAL APPLICATION

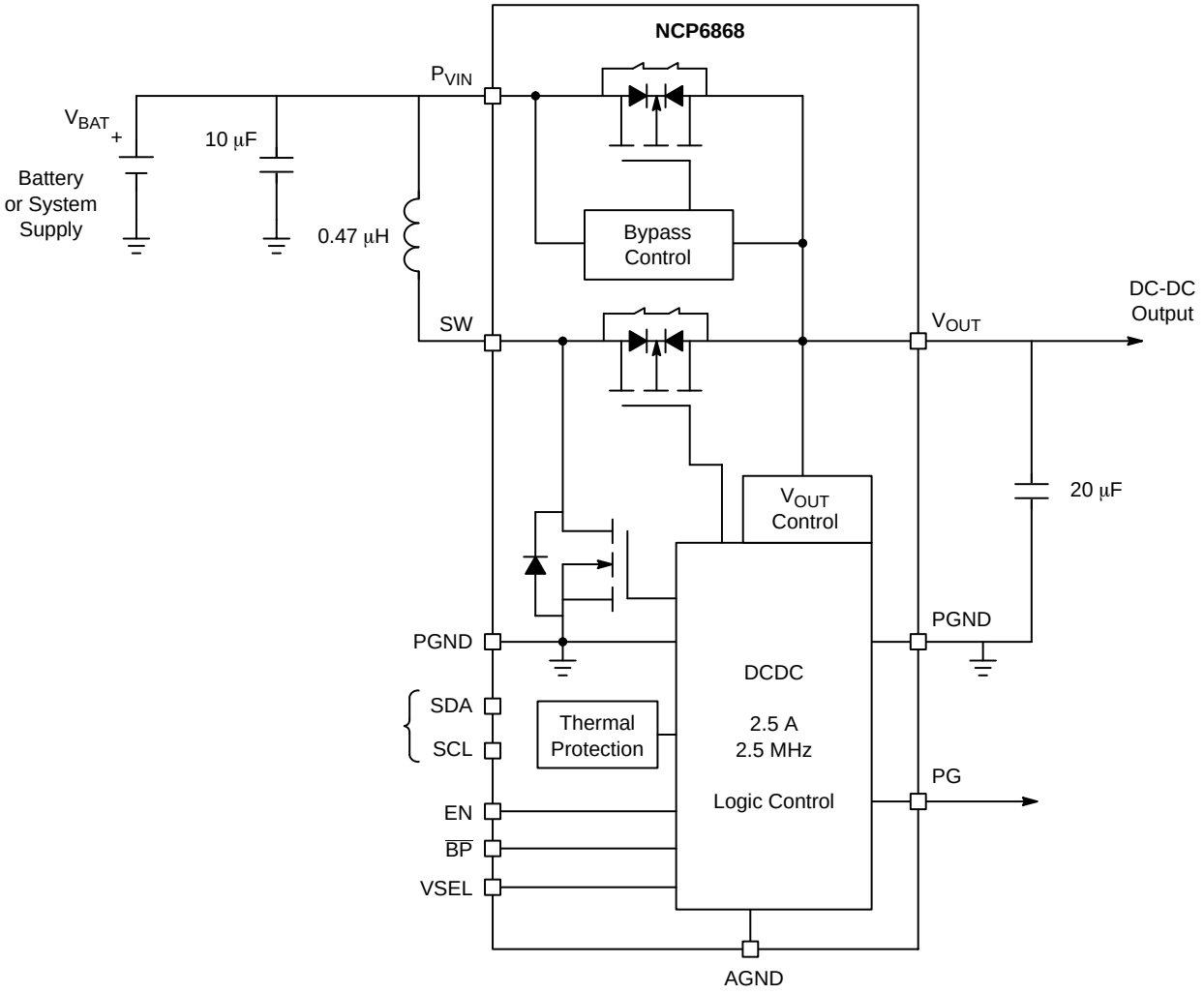


Figure 1. Application Block Diagram

PIN OUT

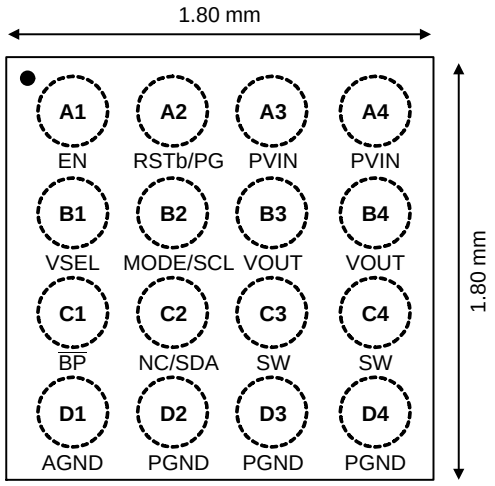


Figure 2. Pin Out (Top View)

Table 1. PIN FUNCTION DESCRIPTION

Pin	Name	Type	Description
A1	EN	Input	Enable Control. Active high will enable the part. There is an internal pull down resistor on this pin.
A2	RSTb/PG	Input/Output	RSTb: drive the A2 pin Low resets all the registers to their default values. RSTb is active when EN Low, not active when EN High. PG: Interrupt Output pin active Low (Open drain); PG is pulled low if a PG event is detected that is output out of regulation, over-voltage, overload, UVLO or TWRN protection is activated. PG is pulled-up High when EN is Low.
A3−A4	P_{VIN}	Power Input	DCDC Input Power connected to the Li-Ion battery. This pin must be decoupled to ground by a 10 μF and 1 μF ceramic capacitors. These capacitors should be placed as close as possible to this pin.
B1	VSEL	Input	Output Voltage Select. This pin can be used to select output voltage when the device operates in boost mode. VSEL = Low, Low voltage target selected; VSEL = High, High voltage target selected. There is an internal pull-down resistor on this pin.
B2	MODE/SCL	Input	MODE: B2 pin is configured as a MODE pin when I^2C is disabled and device output voltage is fixed. When MODE = Low the device is operating in auto mode. This pin must be set Low during device start-up. When MODE = High the device is operating in forced CCM mode. SCL: I^2C interface Clock line when I^2C interface enabled. There is an internal pull down resistor on this pin.
C2	NC/SDA	Ground or Input/Output	Connected to AGND or SDA, I^2C interface Bi-directional Data line. There is an internal pull down resistor on this pin; it is recommended to connect it to AGND if not used. I^2C programming is performed prior to enable the device using the EN pin.
D1	AGND	Ground	Analog Ground. Analog and digital circuit blocks' ground. Must be connected to the system ground.
B3−B4	V_{OUT}	Power Output	Output voltage. Connect Cout as close as possible to the device.
C1	$\overline{BP}$	Input	Bypass pin. Active Low. This pin is used to force the bypass mode. Bypass and High Side transistors are turned On. There is an internal pull-up resistor on this pin.
C3−C4	SW	Power	DC-DC Switch Power pin. This pin connects the power transistors to one end of the inductor. Typical application (2.5 MHz) uses 0.470 μH inductor; refer to application section for more information.
D2−D4	PGND	Ground	Power Ground. Switch Ground. This pin is the power ground and carries the high switching current. High quality ground must be provided to prevent noise spikes. To avoid high-density current flow in a limited PCB track, a local ground plane that connects all PGND pins together is recommended. Analog and power grounds should only be connected together in one location through a printed trace.

Table 2. MODES OF OPERATION

EN	$\overline{BP}$	Device State
0	X	All bias circuits are off and the device is in shutdown mode. During shutdown, current flow is prevented from P_{VIN} to V_{OUT} and from SW to V_{OUT}.
1	0	The device is active and forced in bypass mode. A short circuit protection is embedded in order to prevent the output voltage going to low.
1	1	The device will switch between Boost mode and Bypass mode automatically.

Table 3. MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Analog and Power Pins: P_{VIN}, SW	V_A	−0.3 to +6.0	V
V_{OUT} Pin	V_{OUT}	−0.3 to +6.0	V
Digital pins: EN, VSEL, $\overline{BP}$, MODE/SCL, SDA, PG: Input Voltage Input Current	 V_{DG} I_{DG}	 −0.3 to V_A + 0.3 ≤ 6.0 10	 V mA
Operating Ambient Temperature Range	T_A	−40 to +85	°C
Operating Junction Temperature Range (Note 1)	T_J	−40 to +125	°C
Storage Temperature Range	T_{STG}	−65 to + 150	°C
Maximum Junction Temperature	T_{JMAX}	−40 to +150	°C
Thermal Resistance Junction-to-Ambient (Note 2)	$R_{\Theta JA}$	78	°C/W
Thermal Resistance Junction-to-Board (Note 2)	$R_{\Theta JB}$	13	°C/W
ESD, Electrostatic Discharge Protection, Human Body Model (Note 3) Charged Device Model	 HBM CDM	 2 1	kV
Moisture Sensitivity (Note 4)	MSL	Level 1	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. The thermal shutdown set to 150°C (typical) avoids potential irreversible damage on the device due to power dissipation.
2. The Junction-to-Ambient and Junction-to-Board thermal resistances are a function of Printed Circuit Board (PCB) layout and application. These data are measured using 4-layer PCBs (2s2p). For a given ambient temperature T_A it has to be pay attention to not exceed the max junction temperature T_{JMAX}.
3. Human Body Model per JESD22−A114, Charge Device Model per JESD22−C101
4. Moisture Sensitivity Level (MSL): 1 per IPC/JEDEC standard: J−STD−020A.

Table 4. RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
P_{VIN}	Power Supply (Note 5)			2.35	−	5.5	V
V_{OUT}	V_{OUT} Range			2.85	−	5.3	V
V_{OUT}	Fixed Output Voltage for Standard Versions Other Output Voltages in the Range 3 V to 5.3 V are Available Under Request.	NCP6868V300	VSEL = Low	−	3.00	−	V
			VSEL = High	−	3.20	−	V
		NCP6868V315	VSEL = Low	−	3.15	−	V
			VSEL = High	−	3.35	−	V
		NCP6868V330	VSEL = Low	−	3.30	−	V
			VSEL = High	−	3.50	−	V
		NCP6868V350	VSEL = Low	−	3.50	−	V
			VSEL = High	−	3.70	−	V
		NCP6868V360	VSEL = Low	−	3.60	−	V
			VSEL = High	−	3.80	−	V
		NCP6868V370	VSEL = Low	−	3.70	−	V
			VSEL = High	−	3.90	−	V
		NCP6868V450	VSEL = Low	−	4.50	−	V
			VSEL = High	−	4.70	−	V
		NCP6868V500	VSEL = Low	−	5.00	−	V
			VSEL = High	−	5.20	−	V
I_{OUT}	Continuous Output Current	For V_{OUT} ≤ 3.5 V and P_{VIN} ≥ 2.5 V		0	−	2.5	A
$I_{LoadStartMax}$	Maximum Load Current during Start-up			500			mA
L	Inductor for DCDC Converter (Note 6)			−	0.47	−	μH
C_o	Output Capacitor for DCDC Converter (Note 6)			15	20	56	μF
C_{in}	Input Capacitor for DCDC Converter (Note 6)			3.3	4.7	−	μF

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

5. Operation above 5.5 V input voltage for extended period may affect device reliability.
6. Including de-ratings (refer to application information section of this document for further details)

ELECTRICAL CHARACTERISTICS

Min & Max Limits apply for T_J up to +125°C unless otherwise specified. P_{VIN} = 2.35 V to V_{OUT} (Unless otherwise noted). Typical values are referenced to P_{VIN} = 3.0 V, T_A = +25°C and default configuration (Figure 1) (Note 7)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
SUPPLY CURRENT: PIN P_{VIN}							
I_{QBP}	Operating Quiescent Current, By-Pass Mode (Auto)	V_{OUT} = 3.5 V, P_{VIN} = 3.6 V		−	25	50	μA
I_{QBoost}	Operating Quiescent Current, Boost Mode	V_{OUT} = 3.5 V, P_{VIN} = 3.2 V		−	50	70	μA
I_{SD}	Shutdown Current	EN = Low, P_{VIN} = 3.0 V		−	1	5	μA
$I_{QBPForced}$	Forced By-Pass Mode	V_{OUT} = 3.5 V, P_{VIN} = 3.5 V	Low IQ	−	4	10	μA
		V_{OUT} = 3.5 V, P_{VIN} = 3.5 V	OCP ON	−	15	40	μA
DCDC CONVERTER							
P_{VIN}	Input Voltage Range			2.35	−	5.5	V
V_{OUT_ACC}	Output Voltage Accuracy	Referred to GND, DC, V_{OUT} – P_{VIN} > 100 mV		−2	−	4	%
I_{OUTMAX}	Boost Mode	For $V_{OUT} \le$ 3.5 V and $P_{VIN} \ge$ 2.5 V		−	−	2.5	A
$P_{VINmin2.5A}$	Minimum P_{VIN} for 2.5 A load	V_{OUT} = 3.5 V, T_j < 120°C		−	2.5	−	V
		V_{OUT} = 3.15 V, T_j < 120°C		−	2.35	−	V
$P_{VINmin2A}$	Minimum P_{VIN} for 2A load	V_{OUT} = 5.0 V, T_j < 120°C		−	3.0	−	V
		V_{OUT} = 4.5 V, T_j < 120°C		−	2.8	−	V
$I_{LKout-in}$	V_{OUT} to P_{VIN} Reverse Leakage Current	V_{OUT} = 5 V, EN = Low		−	0.2	1	μA
I_{LKout}	V_{OUT} Leakage Current	V_{OUT} = 0 V, EN = Low, P_{VIN} = 4.2 V		−	0.1	1	μA
F_{SW}	Switching Frequency	P_{VIN} = 3.0 V, V_{OUT} = 3.35 V, I_{OUT} = 1 A		2	2.5	3	MHz
R_{ONPMOS}	P-Channel MOSFET On Resistance (Synchronous Rectifier)	From SW to V_{OUT}, V_{OUT} = 3.5 V, P_{VIN} = 3.5 V		−	30	60	mΩ
R_{ONNMOS}	N-Channel MOSFET On Resistance (Boost Switch)	From SW to PGND, V_{OUT} = 3.5 V, P_{VIN} = 3.5 V		−	25	50	mΩ
R_{ONBP}	By-Pass P-MOSFET On Resistance	From P_{VIN} to V_{OUT}, V_{OUT} = 3.5 V, P_{VIN} = 3.5 V		−	35	60	mΩ
$LOAD_{TR}$	Load Transient Response	P_{VIN} = 3.0 V, V_{OUT} = 3.5 V, I_{OUT} = 500 to 1500 mA, T_R = T_F = 0.1 μs		−	±4	−	%
I_{PKlim}	Boost Peak Current Limit	P_{VIN} = 2.6 V		−	5.0	9.0	A
I_{SS_PKlim}	Boost Peak Current Limit at Soft-Start	P_{VIN} = 2.6 V		−	2.0	−	A
ISS_{PK}	Soft-Start Input Peak Current Limit			−	1600	−	mA
Tss	Soft-Start EN High to Regulation	50 Ω Load, C_{out} = 2 x 10 μF		−	400	500	μs

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

7. Guaranteed by characterization and design.

ELECTRICAL CHARACTERISTICS

Min & Max Limits apply for T_J up to +125°C unless otherwise specified. P_{VIN} = 2.35 V to V_{OUT} (Unless otherwise noted). Typical values are referenced to P_{VIN} = 3.0 V, T_A = +25°C and default configuration (Figure 1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
CONTROL PINS: EN, $\overline{BP}$, VSEL						
V_{IH}	Positive Going Input High Voltage Threshold		1.2	–	–	V
V_{IL}	Negative Going Input Low Voltage Threshold		–	–	0.4	V
R_{PDown}	Pull Down Internal Resistor at Control Pins (EN & VSEL)		–	300	–	kΩ
POWER GOOD PIN: PG						
V_{OLPG}	Power Good Pin Low Voltage Level	I_{PG} = 5 mA	–	–	0.4	V
ILK_{PG}	Power Good Pin Leakage Current	V_{PG} = 5 V	–	–	1	μA
PROTECTIONS FEATURES						
V_{UVLO_Fall}	Under Voltage Lockout Threshold	P_{VIN} Falling	2.25	2.30	2.35	V
V_{UVLO_Rise}	Under Voltage Lockout Threshold	P_{VIN} Rising	2.5	2.6	2.65	V
$V_{UVLOHys}$	Under Voltage Lockout Hysteresis		–	300	–	mV
V_{OVP}	Output Over-Voltage Protection Threshold		–	5.7	6.0	V
V_{OVPhys}	Output Over-Voltage Protection Hysteresis		–	250	–	mV
T_{PGact}	PG Pin Activation Temperature Threshold (TWARN)		–	120	–	°C
T_{PGrel}	PG Pin Release Temperature Threshold		–	100	–	°C
T_{SD}	Thermal Shut Down Protection		–	150	–	°C
T_{SDH}	Thermal Shut Down Hysteresis		–	20	–	°C
t_{RST}	Fault Restart Timer		–	20	–	ms

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL OPERATING CHARACTERISTICS (SUPPLY CURRENTS)

V_{OUT} = 3.5 V, L = 0.47 μH, C_{OUT} = 2 × 22 μF, C_{IN} = 10 μF, T_A = 25°C (unless otherwise noted)

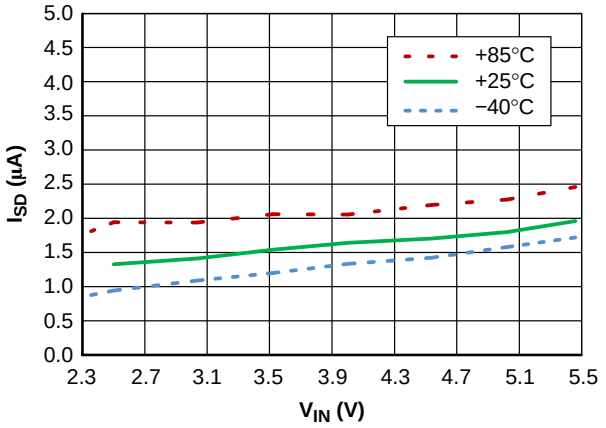


Figure 3. Shutdown Current vs Input Voltage

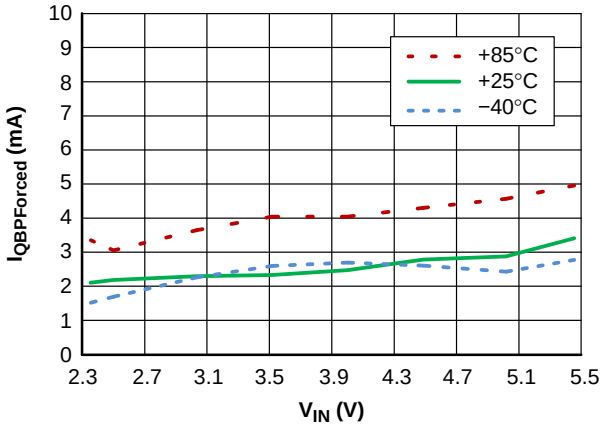


Figure 4. Quiescent Current in Forced Bypass Mode (OCP OFF) vs Input Voltage

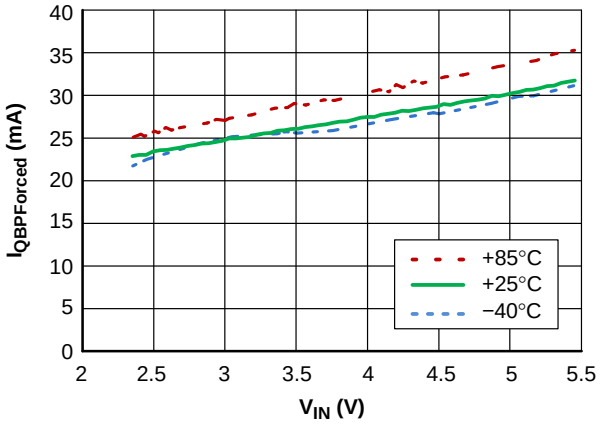


Figure 5. Quiescent Current in Forced Bypass Mode (OCP ON) vs Input Voltage

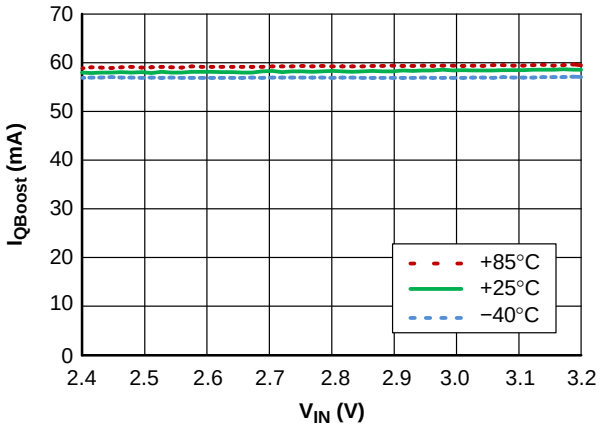


Figure 6. Boost Quiescent Current vs Input Voltage

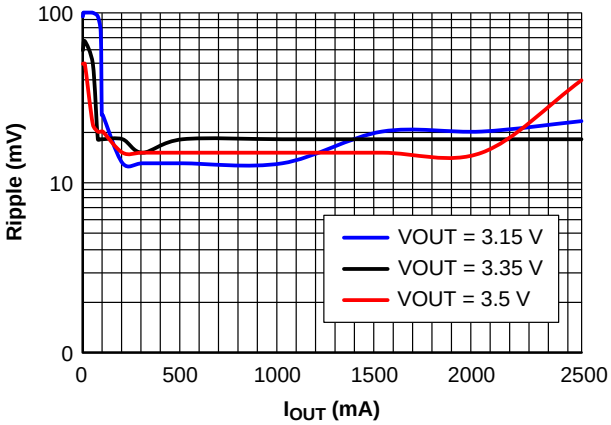


Figure 7. V_{OUT} Ripple vs Output Current

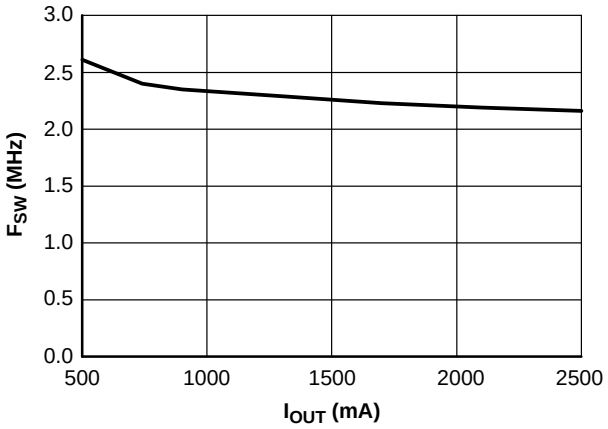


Figure 8. Frequency vs I_{OUT} for V_{OUT} = 3.35 V

TYPICAL OPERATING CHARACTERISTICS (EFFICIENCY)

L = 0.47 μH, C_{OUT} = 2 × 22 μF, C_{IN} = 10 μF, T_A = 25°C (unless otherwise noted)

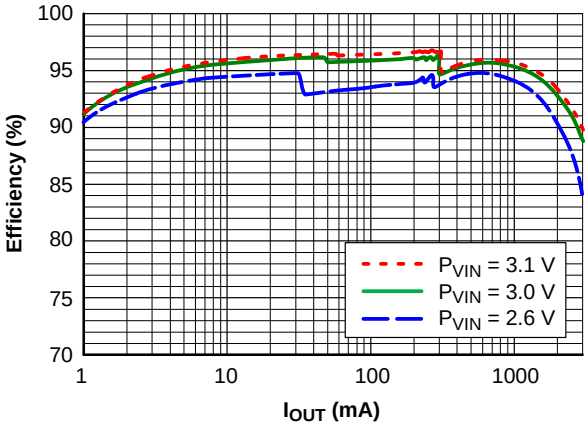


Figure 9. Efficiency vs Output Current, P_{VIN} with V_{OUT} = 3.5 V

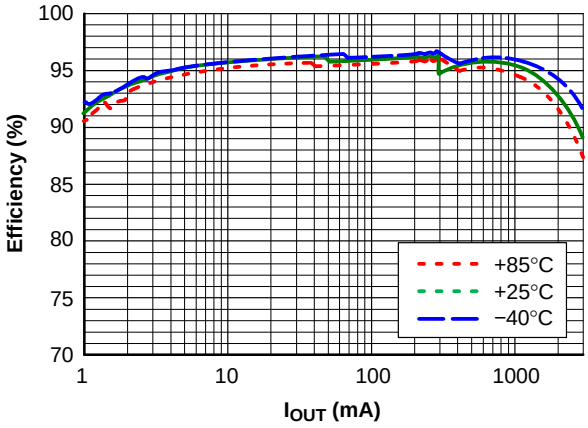


Figure 10. Efficiency vs Output Current and Temperature P_{VIN} = 3.0 V and V_{OUT} = 3.5 V

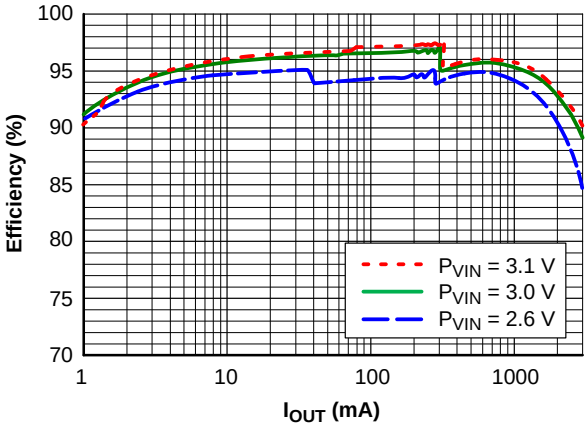


Figure 11. Efficiency vs Output Current, P_{VIN} with V_{OUT} = 3.35 V

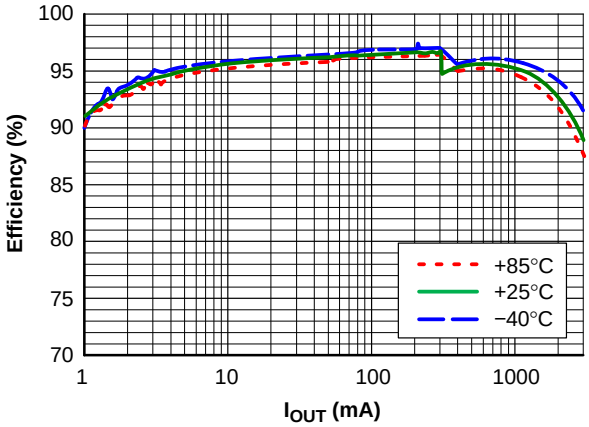


Figure 12. Efficiency vs Output Current and Temperature P_{VIN} = 3.0 V and V_{OUT} = 3.35 V

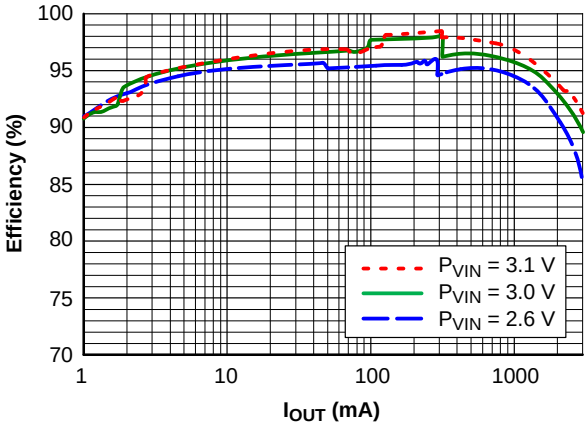


Figure 13. Efficiency vs Output Current, P_{VIN} with V_{OUT} = 3.15 V

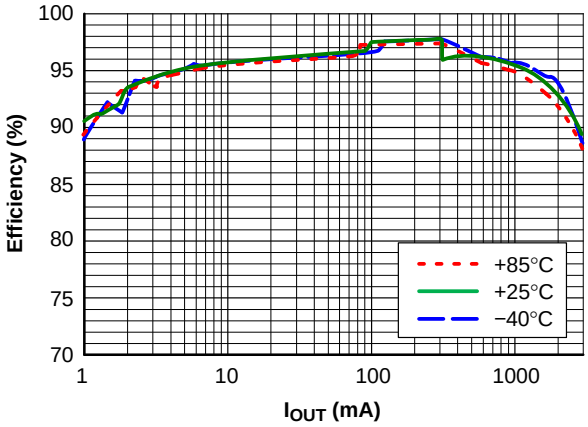


Figure 14. Efficiency vs Output Current and Temperature P_{VIN} = 3.0 V and V_{OUT} = 3.15 V

TYPICAL OPERATING CHARACTERISTICS (START UP AND SHUT DOWN)

P_{VIN} = 3.0 V, L = 0.47 μH, VSEL = 0, C_{OUT} = 2 × 22 μF, C_{IN} = 10 μF, T_A = 25°C (unless otherwise noted)

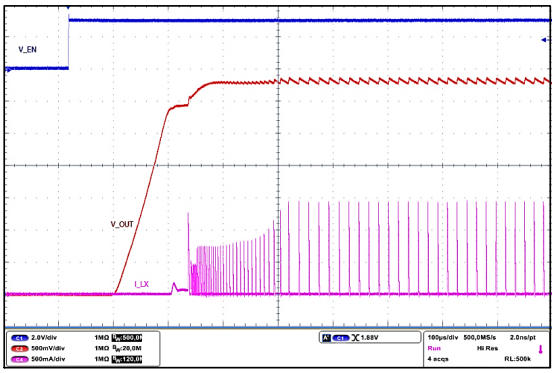


Figure 15. Power-up Response, 50 Ω Load, V_{OUT} = 3.3 V

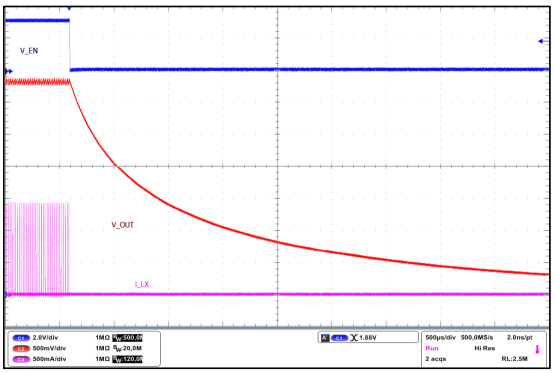


Figure 16. Power-down Response, 50 Ω Load, V_{OUT} = 3.3 V

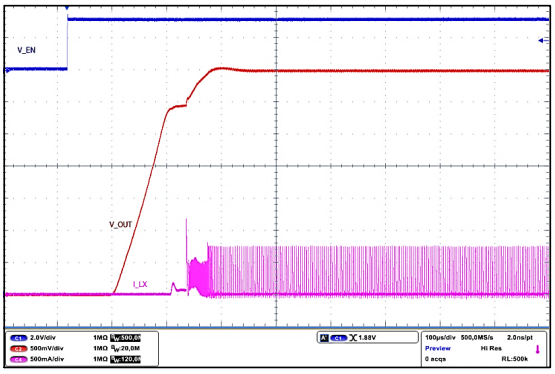


Figure 17. Power-up Response, 50 Ω Load, V_{OUT} = 3.5 V

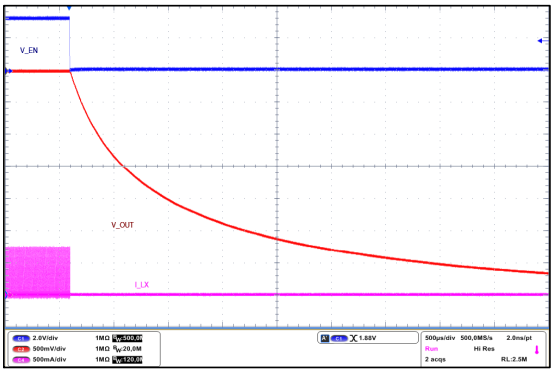


Figure 18. Power-down Response, 50 Ω Load, V_{OUT} = 3.5 V

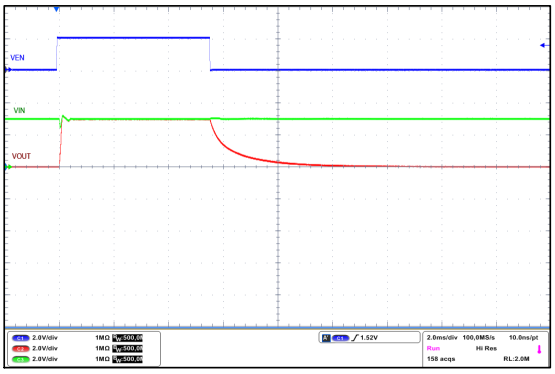


Figure 19. Power-up/down Response in Forced Bypass Mode, V_{IN} = 3.0 V, 25 Ω Load

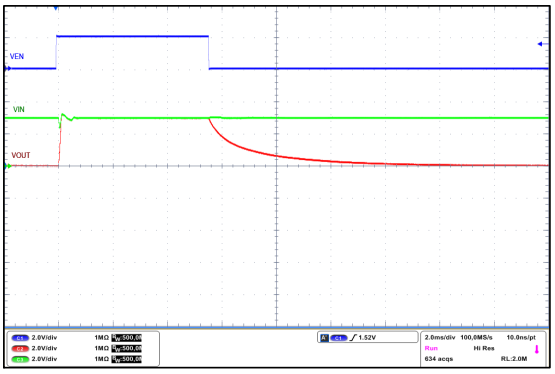


Figure 20. Power-up/down Response in Forced Bypass Mode, V_{IN} = 3.0 V, 50 Ω Load

TYPICAL OPERATING CHARACTERISTICS (DYNAMIC TRANSITION)

P_{VIN} = 3.0 V, L = 0.47 μH, VSEL = 0, C_{OUT} = 2 × 22 μF, C_{IN} = 10 μF, T_A = 25°C (unless otherwise noted)

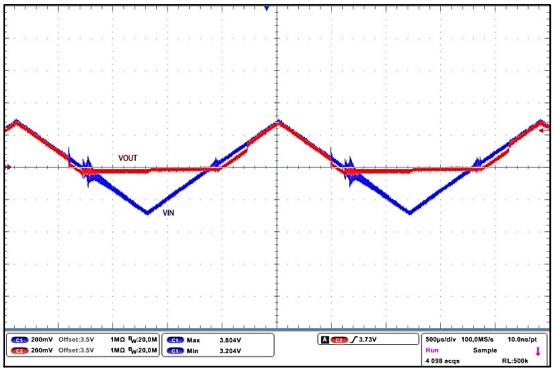


Figure 21. Bypass Entry/Exit, Slow P_{VIN} Ramp 1 ms Edge P_{VIN} = 3.2 V to 3.8 V, I_{OUT} = 500 mA & V_{OUT} = 3.5 V

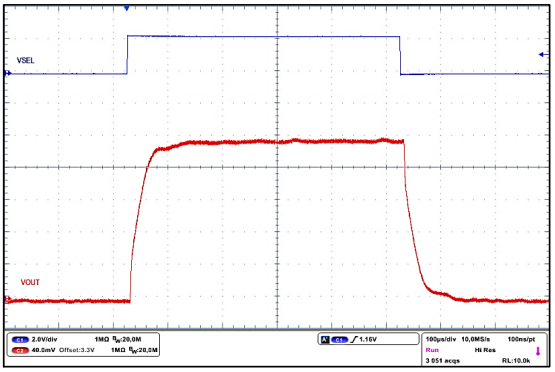


Figure 22. VSEL Step P_{VIN} = 3 V, I_{OUT} = 500 mA & V_{OUT} = 3.5 V <–> 3.7 V

TYPICAL OPERATING CHARACTERISTICS (LOAD TRANSIENT RESPONSES)

L = 0.47 μH, VSEL = 0, C_{OUT} = 2 × 10 μF, C_{IN} = 10 μF, T_A = 25°C (unless otherwise noted)

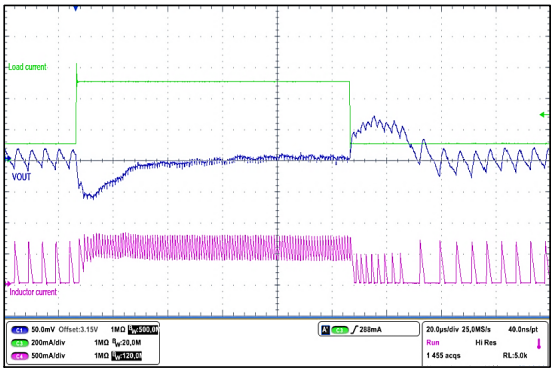


Figure 23. Load Transient Response I_{OUT} = 100 to 500 mA, 100 ns Edge, P_{VIN} = 3 V & V_{OUT} = 3.15 V

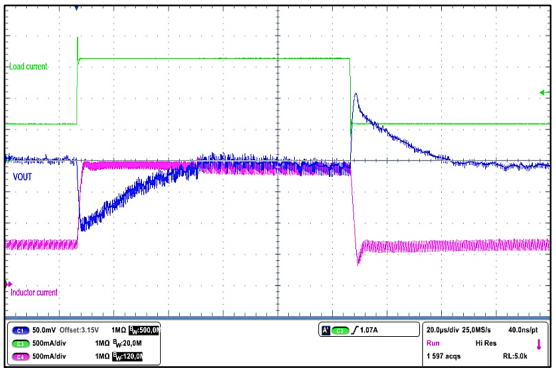


Figure 24. Load Transient Response I_{OUT} = 500 to 1500 mA, 100 ns Edge, P_{VIN} = 3 V & V_{OUT} = 3.15 V

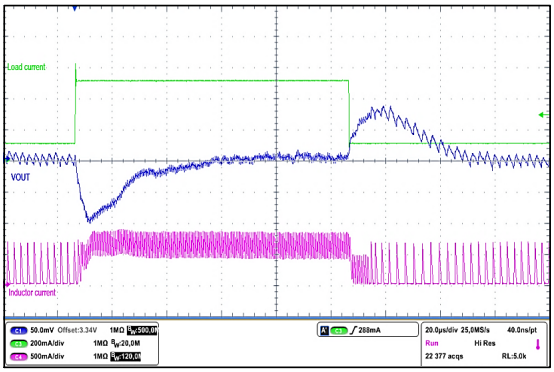


Figure 25. Load Transient Response I_{OUT} = 100 to 500 mA, 100 ns Edge, P_{VIN} = 2.8 V & V_{OUT} = 3.35 V

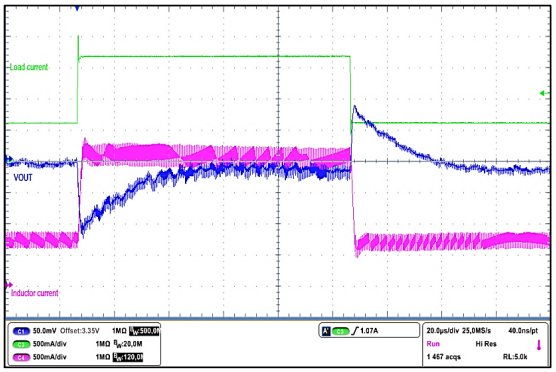


Figure 26. Load Transient Response I_{OUT} = 500 to 1500 mA, 100 ns Edge, P_{VIN} = 2.8 V & V_{OUT} = 3.35 V

TYPICAL OPERATING CHARACTERISTICS (LINE TRANSIENT RESPONSES)

V_{OUT} = 3.5 V, L = 0.47 μH, VSEL = 0, C_{OUT} = 2 × 22 μF, C_{IN} = 10 μF, T_A = 25°C (unless otherwise noted)

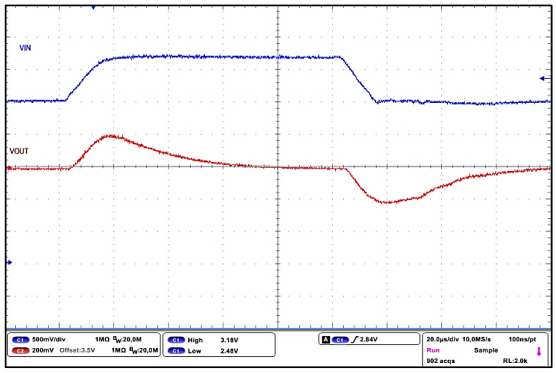


Figure 27. Line Transient Response
V_{IN} = 2.5 V to 3.1 V, 10 μs Edge, 500 mA Load

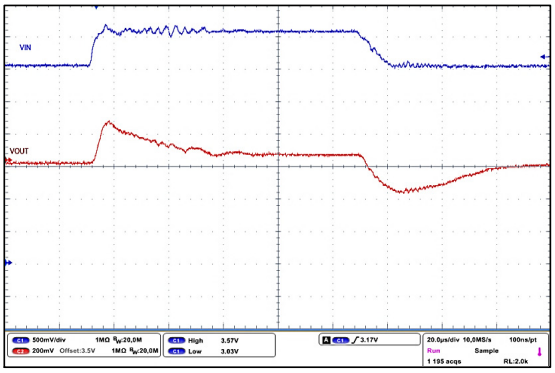


Figure 28. Line Transient Response
V_{IN} = 3.0 V to 3.6 V, 10 μs Edge, 500 mA Load

OPERATING DESCRIPTION

General Description

The NCP6868 is a standalone synchronous step-up converter. It is designed primarily to boost new generation Low-Voltage Li-Ion Batteries (silicon anode-like) embedded into cell and smart phones. The function is to maintain a minimum output voltage even in the case for which the battery voltage is below the system minimum. The device is capable to drive a load up to 2.5 A continuous when P_{VIN} = 2.5 V and V_{OUT} = 3.5 V and operates at a switching frequency in the range of 2.5 MHz in Continuous Conduction Mode (CCM). The device features a Boost mode coupled with a Bypass mode. The Bypass mode is activated when P_{VIN} is above the boost regulator's V_{OUT} set-point (Low or High value set-point adjusted through VSEL pin).

In order to reduce the required V_{OUT} supply difference between heavy and light load the V_{OUT} voltage can be adjusted through VSEL for anticipating a heavy load transition. This allows optimizing power consumption during wide load transitions. The Bypass mode can be forced by dropping the pin $\overline{BP}$ Low.

Boost Mode

The NCP6868 implements an architecture allowing the device to operate in Continuous Conduction Mode (CCM) and Discontinuous Conduction Mode (DCM) modes achieving smoother changes between CCM and DCM. The implemented boost architecture improves transient behavior allowing the boost converter to feature very good transient response.

The NCP6868 operates in DCM in order to save power and improve efficiency at low loads by reducing the switching frequency. When load increases and current in inductor becomes continuous, the controller automatically turns to CCM mode and goes back in DCM when current in the inductor is discontinuous.

By-Pass Operating Mode

The NCP6868 has been designed to manage conditions for which P_{VIN} or V_{BAT} becomes close to the required V_{OUT} output voltage. In that case the NCP6868 enters automatically Bypass Operating mode (or wire mode) from Boost mode. To this end a specific low resistance on-state Bypass (BP) MOSFET is included and activated while the boost converter N-MOSFET is set off. The output voltage is the copy of the input voltage minus a drop-out voltage resulting from the resistance of the BP MOSFET in parallel with the rectifier P-MOSFET plus the inductor: the consequence is a resulting resistance from P_{VIN} to V_{OUT} smaller than the available one (P-MOSFET + inductor) when in Boost mode at 100% duty cycle. In that specific case the Bypass mode offers a better efficiency.

It is possible to force the By-Pass mode by setting the pin $\overline{BP}$ Low.

Shutdown State

The NCP6868 enters shutdown state when setting the EN pin Low (below 0.4 V) or when P_{VIN} drops below its UVLO threshold value (2.3 V typical). The typical current consumption is 1 μA.

Device Power-Up

Applying a voltage above 1.2 V to EN pin will enable the device for normal operation. A soft-start sequence is run when activating EN high. It is recommended when starting up the device to maintain a DC current load below 500 mA. During device enabling current flow is prevented from P_{VIN} to V_{OUT} and conversely from V_{OUT} to P_{VIN}.

Device power up and shutdown operating is detailed on Figure 29.

In the I^2C mode the device is configured and programmed through the I^2C bus once it has been powered up (after Power On Reset) and prior to set the EN pin High. I^2C registers can be reset to default through the RSTb pin without shutdown need. This can be done when EN Low. RSTb not active when EN High.

VSEL Pin

By changing VSEL pin levels, the user has a free way to change the NCP6868's output voltage configuration in regards to the anticipated load or line transitions which can occur, making smoother the output voltage change. The V_{OUT} voltage is increased to the high value target by toggling Low to High the VSEL pin. The output voltage change is stepped to the target value in 20 μs.

Inductor Peak Current Limitations

During normal operation, peak current limitation will monitor and limit the current through the inductor. This current limitation is particularly useful when size and/or height constrain inductor power.

Under-Voltage Lockout (UVLO)

The NCP6868 core does not operate for voltages below the Under Voltage Lock Out (UVLO) level. Below UVLO threshold (typical 2.3 V), all internal circuitries (both analog and digital) are held in reset. NCP6868 operation is not guaranteed down to V_{UVLO} when battery voltage is dropping off. To avoid erratic on/off behavior, a maximum 300 mV hysteresis is implemented. Restart is guaranteed at 2.65 V when V_{BAT} voltage is recovering or rising.

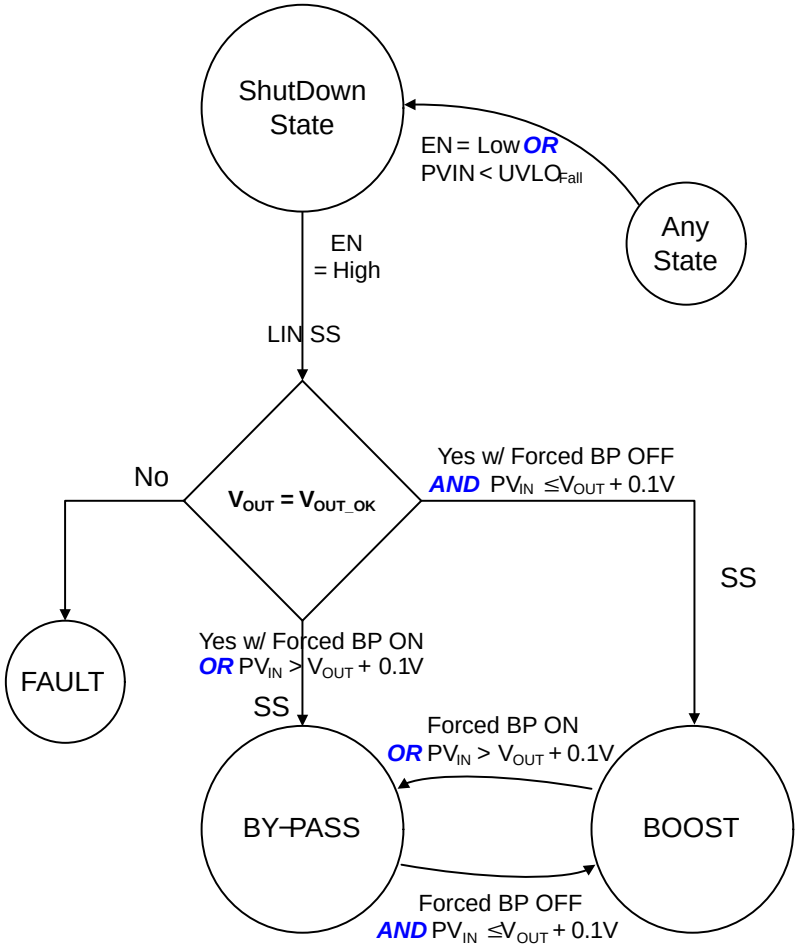


Figure 29. Start-up/Shutdown Diagram

Power Good (PG) Pin and Thermal Management Features

To indicate the output voltage level is established, a power good signal is available. When PG is Low a Power Level fault is flagged, when High Power is Good, this is true when EN is High. In shutdown mode (EN = Low) PG is high.

The power good signal is low when the DC-to-DC converter is off when EN is High (during device starting up or precharge). Once the output voltage reaches 95% of the expected output level, the power good logic signal becomes high and the open drain output becomes high impedance. During operation when the output drops below 90% of the programmed level the power good logic signal goes low (and the open drain signal transitions to a low impedance state) which indicates a power failure. When the voltage rises again to above 95% the power good signal goes high again.

The power-good pin can also be used as an interrupt pin operating as an over-temperature (TPGact/TPGrel), over-load or over-voltage warning function in order to prevent a potential device shutdown resulting respectively from the thermal, overload/short-circuit, or over-voltage protection.

Power Good signal during normal operation can be disabled by clearing the PGDCDC bit in the Configuration Register CONFIG2 bit D3.

Table 5. POWER-GOOD DISABLE-LOW SOURCES

Interrupt Name	Power Good Off Events
POK	Power Good: DC-DC Out of Regulation or Off
TWARN	Thermal Warning (See TPGact & TPGrel)
UVLO	Under Voltage Lock Out
OC	Over-Current (ILIMBP & ILIMBST)
OV	Over-Voltage

Over Current Protection, By-Pass Mode

PG is pulled Low when PMOS current limit has triggered for more than 64 μs, the device shuts down 0 s, 64 μs, 128 μs or 256 μs after depending on the programmed value (BPSCTIMING[1,0]); the shutdown timing is 0 s by default. The device attempts to restart 20 ms after. This will be tried 3 times before definitely shutting down in order to eliminate erratic events due to negative spikes on V_{OUT}.

Over Current Protection, Boost Mode

In boost mode the current protection enables two mechanisms. When the Ipeak limit is triggered the boost is in a state where it is going to keep regulating for 2 ms, after this period of time the boost converter shuts down immediately. During this period of time if the short circuit is strong and drops the output voltage down to $V_{IN}/2$ then the converter shuts down immediately. So there's a double protection based on an Ipeak detection timing period of 2 ms and voltage drop detection. During this process of short circuit protection the PG pin toggles High to Low when Vout drops below 90% of V_{OUT} target.

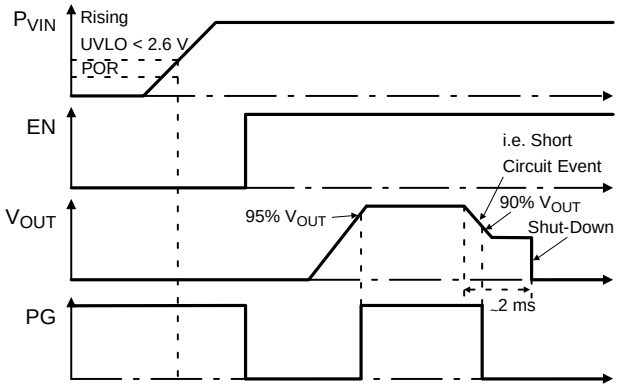


Figure 30. Power Good (PG) Behavior Example

Over-Voltage Protection

PG is pulled Low when the V_{OUT} voltage limit of 5.7 V has triggered for more than 64 μs, the device shuts down after this period of time and attempts to restart 20 ms after. This will be tried 3 times before definitely shutting down in order to eliminate erratic events due to negative spikes on V_{OUT}.

Thermal Shutdown Feature (TSD)

The thermal capability of IC can be exceeded due to boost converter output stage power level. A thermal protection circuitry is therefore implemented to prevent the IC from damage. This protection circuitry is only activated when the core is in active mode (output voltage is turned on). During thermal shutdown, output voltage is turned off and the device enters shutdown mode.

Thermal shutdown threshold is set at 150°C (typical) when the die temperature increases and, in order to avoid erratic on/off behavior, a 20°C hysteresis is implemented. So, after a typical 150°C thermal shutdown, the NCP6868 will return to normal operation when the die temperature cools down to 130°C. This normal operation depends on the input conditions and configuration at the time the device recovers.

Dynamic Voltage Scaling (DVS)

The output voltage change is operated through I^2C or pin VSEL using a Dynamic Voltage Scaling (DVS) approach when the required voltage change is higher than 200 mV (Either by I^2C or VSEL pin). The change between set points is managed in a smooth fashion without disturbing the operation of the device under power.

When programming a more than 200 mV-stepped new output voltage, the output raises in steps of 200 mV every 32 μs typical such that the dV/dt is controlled. The voltage change speed can be programmed with the following values: 32 μs or 64 μs, 32 μs being the default value.

DVS sequence is automatically initiated by changing output voltage settings. There are two ways to change these settings:

- Directly Change the Active Setting Register Value (PROGVOUTLOW [5,0]/PROGVOUTHIGH [5,0] Registers) via I^2C Command
- Change the VSEL Internal Signal Level by Toggling VSEL Pin

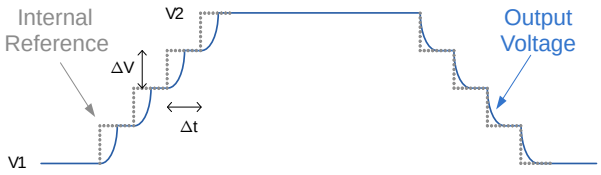


Figure 31. DVS Diagram

Interrupt Control Process (INTSEN1, INTSEN2, INTACK & INTMSK Registers):

The interrupt controller continuously monitors internal interrupt sources, generating an interrupt signal when a system status change is detected (dual edge monitoring).

Individual bits generating interrupts will be set to 1 in the INTACK register (I^2C read only registers), indicating the interrupt source. INTACK register is automatically reset by an I^2C read. The INTSEN1 and INTSEN2 registers (read only register) contains real-time indicators of interrupt sources.

All interrupt sources can be masked by writing in register INTMSK. Masked sources will never generate an interrupt request on PG pin (see Figure 37).

The PG pin is an open drain output. A non masked interrupt request will result in PG pin being driven low.

When the host reads the INTACK registers the PG pin is released to high impedance and the interrupt register INTACK is cleared.

Figure 32 illustrates the Interrupt process.

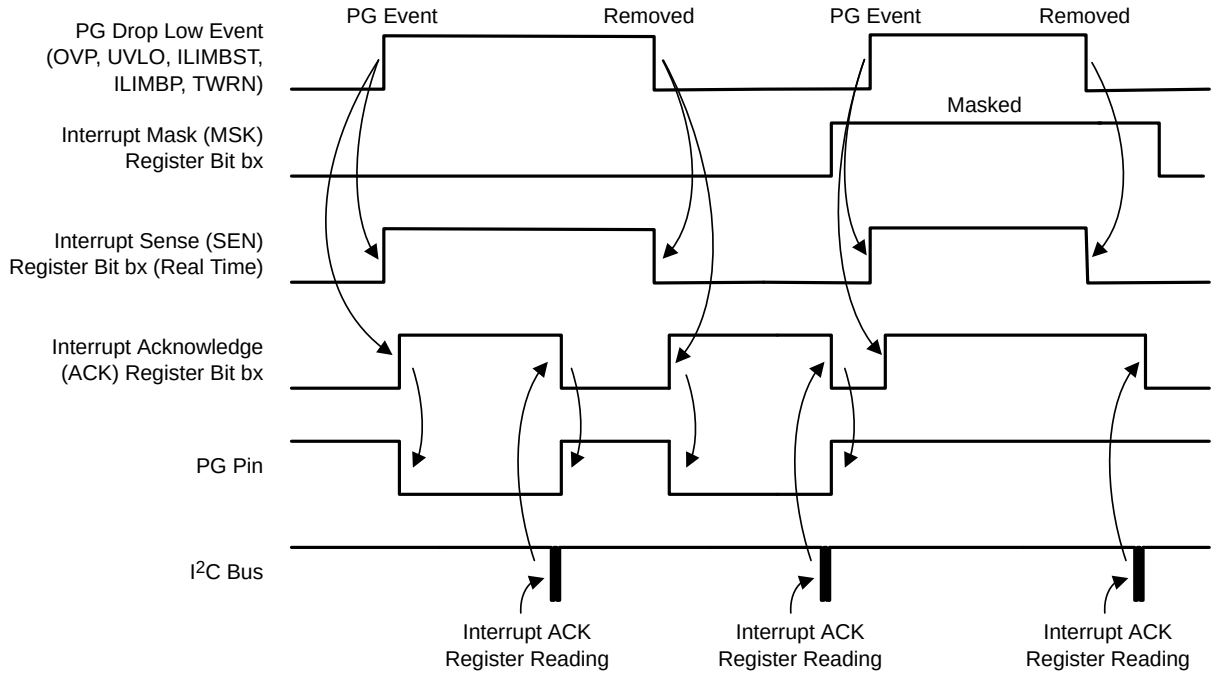


Figure 32. Interrupt Operation Example

I²C Compatible Interface

The NCP6868 can support a subset of I²C protocol detailed below.

The NCP6868 communicates with the external processor by means of a serial link using a 400 kHz up to 3.4 MHz I²C two-wire interface protocol. The I²C interface provided is fully compatible with the Standard, Fast and High-Speed I²C modes. The NCP6868 is not intended to operate as a master controller. It is under the control of the main controller (master device), which controls the clock (pin SCL) and the read or write operations through SDA. The I²C bus is an addressable interface (7-bit addressing only) featuring two Read/Write addresses.

I²C Communication Description

The first byte transmitted is the Chip address (with the LSB bit set to 1 for a read operation, or set to 0 for a Write operation). The following data will be:

- In case of a Write operation, the register address (@REG) pointing to the register we want to write is followed by the data we will write in that location. The writing process is auto-incremental, so the first data will be written in @REG, the contents of @REG are incremented and the next data byte is placed in the location pointed to by @REG + 1…, etc.
- In case of read operation, the NCP6868 will output the data from the last register that has been accessed by the last write operation. Like the writing process, the reading process is auto-incremental.

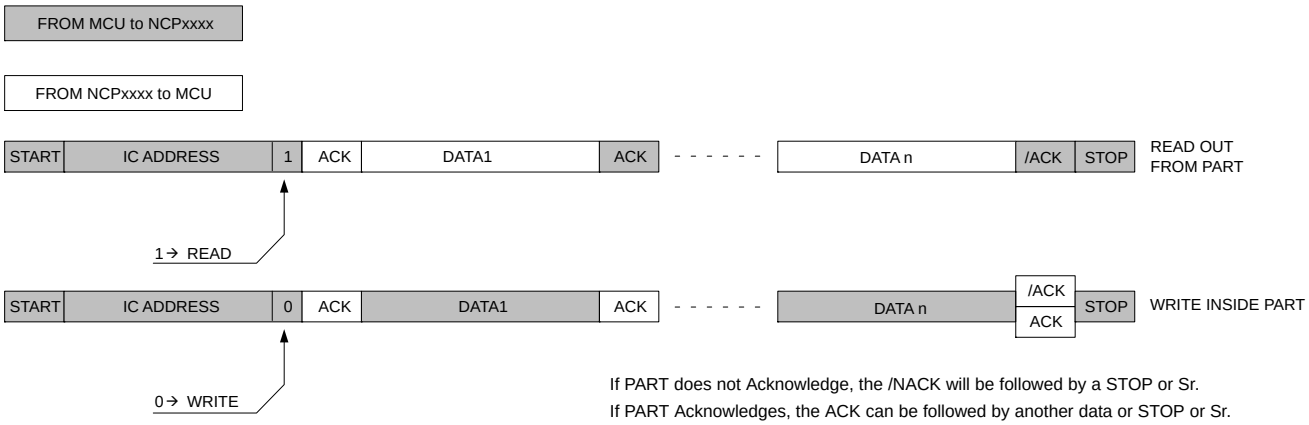


Figure 33. General Protocol Description

Read Out from Part

The Master will first make a “Pseudo Write” transaction with no data to set the internal address register. Then, a stop then start or a Repeated Start will initiate the read transaction from the register address the initial write transaction has pointed to:

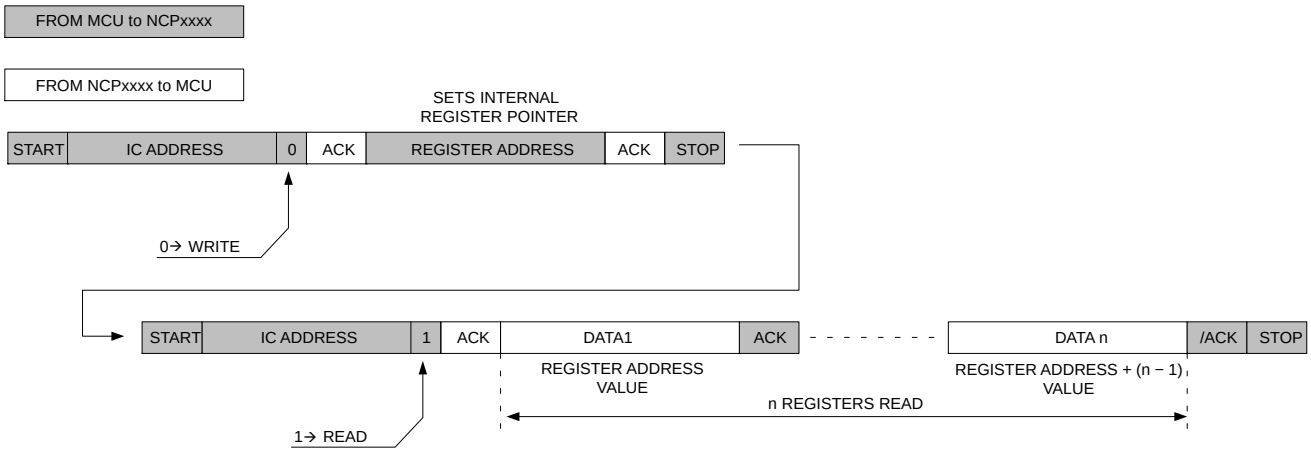


Figure 34. Read Out from Part

The first WRITE sequence will set the internal pointer to the register we want access to. Then the read transaction will start at the address the write transaction has initiated.

Transaction with Real Write then Read

With Stop then Start

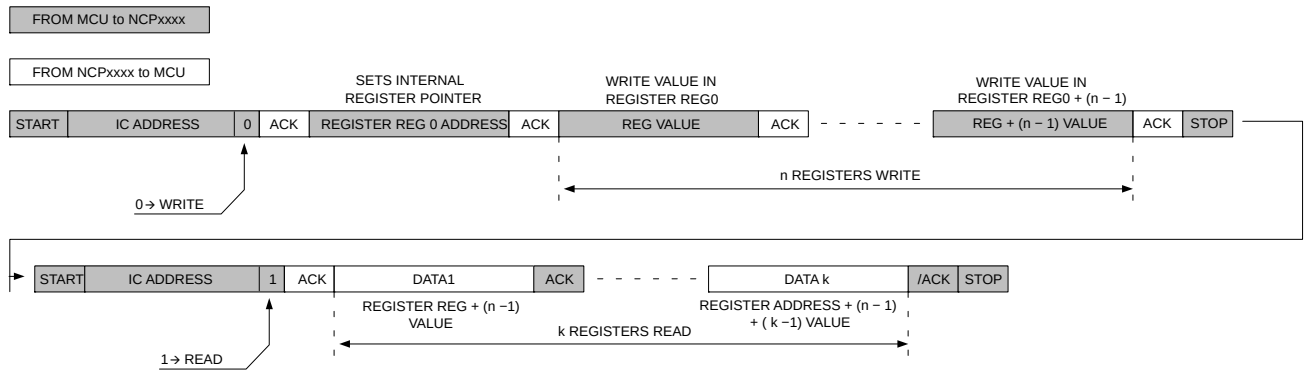


Figure 35. Write Followed by Read Transaction

Write in Part

Write operation will be achieved by only one transaction. After chip address, the MCU first data will be the internal register we want access to, then following data will be the data we want to write in Reg, Reg + 1, Reg + 2, …, Reg + n.

Write n Registers:

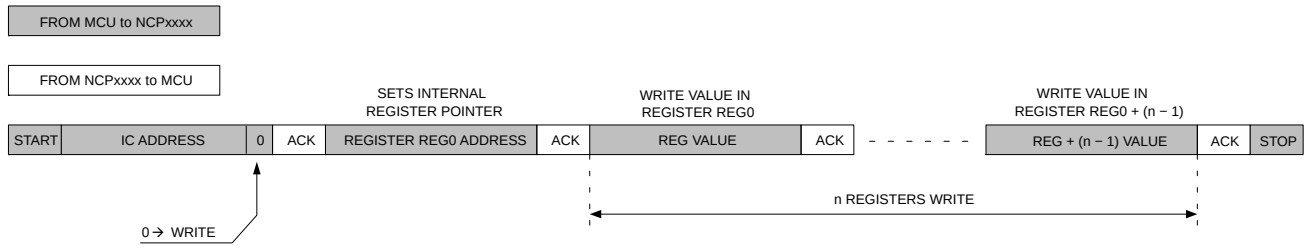


Figure 36. Write in n Registers

I²C Address

NCP6868 has four available I²C address selectable by factory settings (ADD0 to ADD3). Different address settings can be generated upon request to ON Semiconductor. The default address is set to ECh/EDh.

Table 6. I²C ADDRESS

I²C Address	Hex	A7	A6	A5	A4	A3	A2	A1	A0
ADD0	W 0xE8; R 0xE9	1	1	1	0	1	0	0	R/W
ADD1	W 0xEA; R 0xEB	1	1	1	0	1	0	1	R/W
ADD2 (Default)	**W 0xEC; R 0xED**	**1**	**1**	**1**	**0**	**1**	**1**	**0**	**R/W**
ADD3	W 0xEE; R 0xEF	1	1	1	0	1	1	1	R/W

Register Map

Table 7 describes I²C registers.

Registers can be:

R: Read Only Register

RC: Read then Clear (Dual Edge)

R/W: Read and Write Register

Reserved: Address is Reserved and Register is Not Physically Designed

Spare: Address is Reserved and Register is Physically Designed

Table 7. I²C REGISTERS MAP DESCRIPTION

Address	Register Name	Type	Default	Function
00h	RID	R	00h	Revision Identification
01h	CONFIG	R/W	00h	Configuration Programming
02h	PROGVOUT_LOW	R/W	09h	VOUT Programming when VSEL = Low
03h	PROGVOUT_HIGH	R/W	0Dh	VOUT Programming when VSEL = High
04h	ILIM	R/W	03h	Current Limit Programming
05h	INTSEN1	R	00h	Sense Register (Real Time Status Register)
06h	INTSEN2	R	00h	Sense Register (Real Time Status Register)
07h	INTACK	RC	00h	Interrupt Register
08h	INTMSK	R/W	FFh	Mask Register to Enable or Disable Interrupt Sources (Trim)
09h	PID	R	68h	Product Identification
0Ah	FID	R	00h	Features Identification (Trim)
0Bh	CONFIG2	R/W	07h	Configuration Programming 2
0Ch to xxh	–	–	–	Reserved

Registers Description

Table 8. REVISION ID REGISTER

Name: RID				Address: 00h			
Type: R				Default: 00000000b (00h)			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
RID_7	RID_6	RID_5	RID_4	RID_3	RID_2	RID_1	RID_0

Bit	Bit Description
RID[7..0]	Revision Identification 00000000: Silicon Revision 1.0 00000001: Silicon Revision 1.1 00000010: Silicon Revision 1.2 00000100: Silicon Revision 1.3

Table 9. CONFIGURATION REGISTER

Name: CONFIG				Address: 01h			
Type: R/W				Default: 00000000b (00h)			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
FORCERST	ENABLE		Spare = 0			MODE[1,0]	

Bit	Bit Description
MODE	Device Mode of Operation: 0x, 11: Normal Operation, Auto Mode 10: Forced CCM Mode
ENABLE[6:5]	Device Enable Modes: 00: Device Operation Follows Hardware Control Signal (Refer to Table 2) 01: Device Operates in Auto Mode Regardless of the $\overline{BP}$ Pin (EN = 1) 10: Device is Forced in Bypass Mode Regardless of the $\overline{BP}$ Pin Value (EN = 1) 11: Device is in Shutdown Mode. During Shutdown, Current Flow is Prevented from V_{IN} to V_{OUT} and from V_{OUT} to V_{IN}. All Bias Circuits are Off
FORCERST	Force Reset Bit 0: Normal Operation. Self Cleared to 0 1: Force Reset of Internal Registers to Default

Table 10. DC TO DC OUTPUT VOLTAGE PROGRAMMING REGISTER

Name: PROGVOUTLOW				**Address: 02h**			
Type: R/W				**Default: 00001001b (09h)**			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Spare = 0	Spare = 0	PROGVOUTLOW[5:0]					
Bit	**Bit Description**						
PROGVOUT LOW[5:0]	Sets the DC to DC Converter Output Voltage (see Table 11) **Default 00001001b => 3.3 V** (VSEL = 0)						

Table 11. DC TO DC OUTPUT VOLTAGE PROGRAMMING

PROGVOUTLOW[5:0]	**V_{OUT} (V) @ VSEL = 0**
000000b	2.850
000001b	2.900
000010b	2.950
000011b	3.000
000100b	3.050
000101b	3.100
000110b	3.150
000111b	3.200
001000b	3.250
001001b	**3.300**
001010b	3.350
001011b	3.400
001100b	3.450
001101b	3.500
001110b	3.550
001111b	3.600
010000b	3.650
010001b	3.700
010010b	3.750
010011b	3.800
010100b	3.850
010101b	3.900
010110b	3.950
010111b	4.000
011000b	4.050
011001b	4.100
011010b	4.150
011011b	4.200
011100b	4.250
011101b	4.300
011110b	4.350
011111b	4.400
100000b	4.450
100001b	4.500
100010b	4.550
100011b	4.600
100100b	4.650
100101b	4.700
100110b	4.750
100111b	4.800
101000b	4.850
101001b	4.900
101010b	4.950
101011b	5.000
101100b	5.050
101101b	5.100
101110b	5.150
101111b	5.200
110000b	5.250
110001b	5.300

Table 12. DC TO DC OUTPUT VOLTAGE PROGRAMMING REGISTER

Name: PROGVOUTHIGH				**Address: 03h**			
Type: R/W				**Default: 00011001b (0Dh)**			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Spare = 0	Spare = 0	PROGVOUTHIGH[5:0]					
Bit	**Bit Description**						
PROGVOUT HIGH[5:0]	Sets the DC to DC Converter Output Voltage (see Table 13) **Default 00001101b => 3.5 V** (VSEL = 1)						

Table 13. DC TO DC OUTPUT VOLTAGE PROGRAMMING

PROGVOUTHIGH[5:0]	**V_{OUT} (V) @ VSEL = 1**
000000b	2.850
000001b	2.900
000010b	2.950
000011b	3.000
000100b	3.050
000101b	3.100
000110b	3.150
000111b	3.200
001000b	3.250
001001b	3.300
001010b	3.350
001011b	3.400
001100b	3.450
001101b	**3.500**
001110b	3.550
001111b	3.600
010000b	3.650
010001b	3.700
010010b	3.750
010011b	3.800
010100b	3.850
010101b	3.900
010110b	3.950
010111b	4.000
011000b	4.050
011001b	4.100
011010b	4.150
011011b	4.200
011100b	4.250
011101b	4.300
011110b	4.350
011111b	4.400
100000b	4.450
100001b	4.500
100010b	4.550
100011b	4.600
100100b	4.650
100101b	4.700
100110b	4.750
100111b	4.800
101000b	4.850
101001b	4.900
101010b	4.950
101011b	5.000
101100b	5.050
101101b	5.100
101110b	5.150
101111b	5.200
110000b	5.250
110001b	5.300

Table 14. PEAK CURRENT LIMIT REGISTER

Name: ILIM				Address: 04h			
Type: R/W				Default: 00000011 (03h)			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Spare = 0	SCPBP_DIS	ILIM_DIS	Spare = 0	ILIM [3:0]			

Bit	Bit Description
ILIM	Inductor Peak Current Settings (see Table 15)
ILIM_DIS	Enable/Disable Peak Inductor Current Limit 0: Current Limit Enabled 1: Current Limit Disabled
SCPBP_DIS	Enable/Disable Bypass Short Circuit Protection 0: Protection Enabled 1: Protection Disabled

Table 15. DC TO DC PEAK CURRENT LIMIT PROGRAMMING

ILIM[3:0]	Peak Current Setting
0000b	2 A
0001b	3 A
0010b	4 A
0011b	**5 A**
0100b	6 A
0101b	7 A
0110b	8 A
0111b	9 A

Table 16. INTERRUPT SENSE REGISTER 1

Name: INTSEN1				Address: 05h			
Type: R				Default: 00000000b (00h)			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
SEN_TSD	SEN_ TWARN	SEN_ DCDCMODE	SEN_ OPMODE	SEN_ILIMBP	SEN_ ILIMBST	Spare = 0	SEN_POK

Bit	Bit Description
SEN_POK	Power Good Ok Sense **0: DCDC Output Voltage below Target** 1: DCDC Output Voltage within Nominal Range. This Bit is Set if the Converter is Forced in Bypass Mode
SEN_ILIMBST	Current Limit Status Bit (DC-DC Boost Mode): **0: DCDC Output Current is below Limit** 1: DCDC Output Current is over Limit
SEN_ILIMBP	Current Status Bit (Bypass Mode) **0: Bypass Output Current is below Limit** 1: Bypass Output Current is over Limit
SEN_OPMODE	Device Mode of Operation Status Bit: **0: Device Operates in By-Pass Mode** 1: Device Operates in Boost Mode
SEN_DCDCMODE	DC-DC Mode of Operation Status Bit: **0: Device Operates in DCM Mode** 1: Device Operates in CCM Mode
SEN_TWARN	Thermal Warning Sense **0: Junction Temperature below Thermal Warning Limit** 1: Junction Temperature over Thermal Warning Limit
SEN_TSD	Thermal Shutdown Sense **0: Junction Temperature below Thermal Shutdown Limit** 1: Junction Temperature over Thermal Shutdown Limit

Table 17. INTERRUPT SENSE REGISTER 2

Name: INTSEN2				**Address: 06h**			
Type: R				**Default: 00000000b (00h)**			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Spare = 0			SEN_OV	SEN_UVLO	Spare = 0		

Bit	**Bit Description**
SEN_UVLO	Under Voltage Sense **0: Input Voltage Higher than UVLO Threshold** 1: Input Voltage Lower than UVLO Threshold
SEN_OV	Over Voltage Sense **0: Output Voltage Lower than OVP Threshold** 1: Output Voltage Higher than OVP Threshold

Table 18. INTERRUPT ACKNOWLEDGE REGISTER

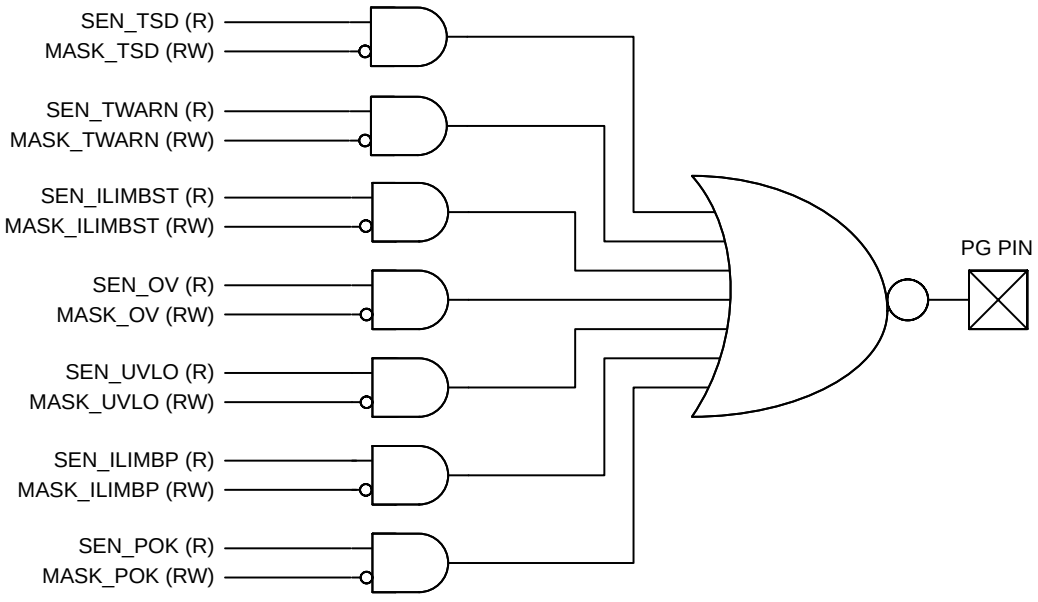
Name: INTACK				**Address: 07h**			
Type: RC				**Default: 00000000b (00h)**			
Trigger: Dual Edge [D7...D0]							
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
ACK_TSD	ACK_ TWARN	ACK_ ILIMBST	ACK_OV	ACK_UVLO	ACK_ILIMBP	Spare = 0	ACK_POK

Bit	**Bit Description**
ACK_POK	Power Good Sense Acknowledgement **0: Cleared** 1: DCDC Power Good Event Detected
ACK_ILIMBP	ByPass Over Current Sense **0: Cleared** 1: ByPass Over Current Limit Detected
ACK_UVLO	Under Voltage Sense Acknowledgement **0: Cleared** 1: Under Voltage Event Detected
ACK_OV	Over Voltage Sense Acknowledgement **0: Cleared** 1: Over Voltage Event Detected
ACK_ILIMBST	DCDC Over Current Sense **0: Cleared** 1: DCDC Over Current Limit Detected
ACK_TWARN	Thermal Warning Sense Acknowledgement **0: Cleared** 1: Thermal Warning Event Detected
ACK_TSD	Thermal Shutdown Sense Acknowledgement **0: Cleared** 1: Thermal Shutdown Event Detected

Table 19. INTERRUPT MASK REGISTER

Name: INTMASK				**Address: 08h**			
Type: RW				**Default: 11111111b (FFh)**			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
MASK_TSD	MASK_ TWARN	MASK_ ILIMBST	MASK_OV	MASK_ UVLO	MASK_ ILIMBP	Spare = 1	MASK_POK

Bit	**Bit Description**
MASK_POK	Power Good Interrupt Source Mask 0: Interrupt is Enabled **1: Interrupt is Masked**
MASK_ILIMBP	DCDC over Current Interrupt Source Mask 0: Interrupt is Enabled **1: Interrupt is Masked**
MASK_UVLO	Under Voltage Interrupt Source Mask 0: Interrupt is Enabled **1: Interrupt is Masked**
MASK_OV	Over Voltage Interrupt Source Mask 0: Interrupt is Enabled **1: Interrupt is Masked**
MASK_ILIMBST	DCDC over Current Interrupt Source Mask 0: Interrupt is Enabled **1: Interrupt is Masked**
MASK_TWARN	Thermal Warning Interrupt Source Mask 0: Interrupt is Enabled **1: Interrupt is Masked**
MASK_TSD	Thermal Shutdown Interrupt Source Mask 0: Interrupt is Enabled **1: Interrupt is Masked**



PG pin will go to low state if the corresponding sense goes to 1 AND if the corresponding mask is cleared.

Figure 37. Interruption Masking Logical Diagram

Table 20. PRODUCT ID REGISTER

Name: PID				**Address: 09h**			
Type: R				**Default: 01101000b (68h)**			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
PID[7:4]				PID[3:0]			
Bit	**Bit Description**						
PID[7..0]	Product Identification 01101000b = 68h w/ PID[7:4] = 6, PID[3:0] = 8						

Table 21. FIRMWARE ID REGISTER

Name: FID				**Address: 0Ah**			
Type: R				**Default: 00000000b (00h)**			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
FID_7	FID_6	FID_5	FID_4	FID_3	FID_2	FID_1	FID_0
Bit	**Bit Description**						
FID[7..0]	Firmware Identification **00000000: Firmware Revision 1.0** 00000001: Firmware Revision 1.1 00000010: Firmware Revision 1.2 00000011: Firmware Revision 1.3 …						

Table 22. CONFIGURATION REGISTER 2

Name: CONFIG2				**Address: 0Bh**			
Type: R/W				**Default: 00000111 (07h)**			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Spare = 0		BPSCTIMING[1,0]		DVSTIMING	PGDCDC	RSTSTATUS	REARM
Bit	**Bit Description**						
REARM	Rearming of Device after TSD 0: No Re-Arming after TSD **1: Re-Arming Active after TSD with No Reset of I^2C Registers: New Power-Up Sequence is Initiated with Previously Programmed I^2C Registers Values**						
RSTSTATUS	Reset Indicator Bit 0: Must be Written to 0 after Register Reset **1: Default (Loaded after Registers Reset)**						
PGDCDC	Power Good Enabling 0 = Disable **1 = Enable**						
DVSTIMING	DVS Timing Change **0 = 200 mV Step / 32 μs** 1 = 200 mV Step / 64 μs						
BPSCTIMING[1,0]	Short-Circuit Protection Activation Delay **00 = 0 s** 01 = 64 μs 10 = 128 μs 11 = 256 μs						

APPLICATION INFORMATION

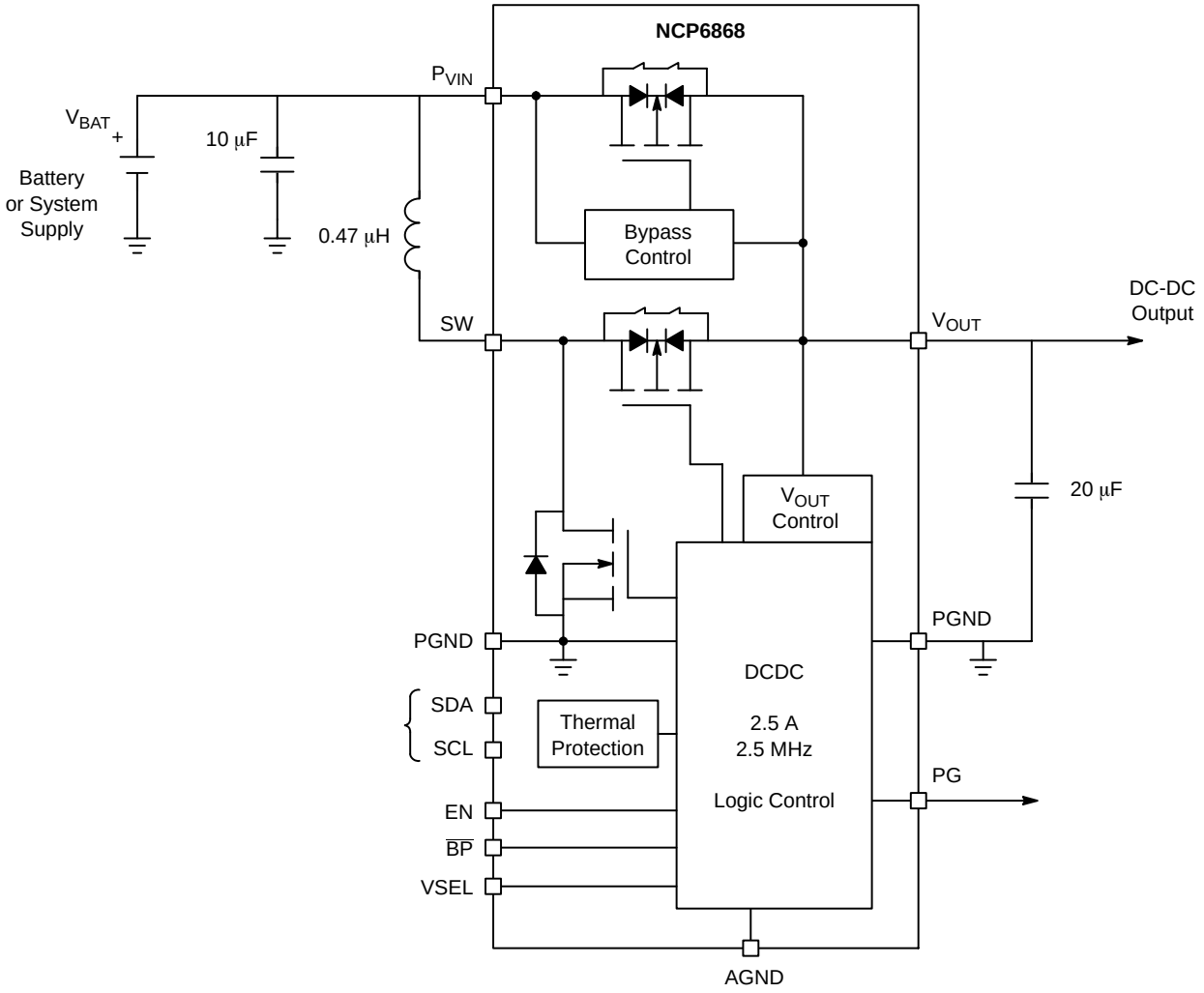


Figure 38. Application Block Diagram

Inductor Selection

The selected inductor must have high enough saturation current rating to be higher than the maximum peak current which can reach 4 A for the default configuration for a short period of time during overload situations. Table 23 shows recommended inductor featuring 0.47 μH of nominal value. Peak-current limit inductor is used.

The inductor also needs to have high enough current rating based on temperature rise concern. Low DCR is good for efficiency improvement and temperature rise reduction.

Table 23. RECOMMENDED INDUCTORS

Supplier	Part #	Value (μH)	Size (L × I × T) (mm)	DC Rated Current (A)	DCR Max @ 25°C (mΩ)
Toko	DFE201610A−R47M−T00	0.47	20 × 16 × 1	4.0	53
Toko	DFE201610P−R47M−T00	0.47	20 × 16 × 1	4.1	41
Toko	DFE201612R−R47M−T00	0.47	20 × 16 × 1.2	4.4	40
Toko	DFE201612P−R47M−T00	0.47	20 × 16 × 1.2	4.9	33
TDK	TFM252010A−R47M	0.47	25 × 20 × 1.0	4.5	30
TDK	TFM252010GHM−R47MTAA	0.47	25 × 20 × 1.0	4.3	26

Output Capacitor Selection

The output capacitor selection is determined by output voltage ripple and load transient response requirement. For high transient load performance high output capacitor value must be used. It is recommended to pay attention to the variation of the capacitor value when the bias voltage across this capacitor varies. Usually the capacitor value decreases with the bias voltage and X5R/X7R low ESR ceramic capacitors are recommended in order to guarantee the effective capacitor value under operating conditions.

Input Capacitor Selection

One of the input capacitor selection guides is the input voltage ripple requirement. To minimize the input voltage ripple and get better decoupling in the input power supply rail, ceramic capacitor is recommended due to low ESR and ESL.

The input capacitor needs also to be sufficient to protect the device from over voltage spike and a minimum of 4.7 μF capacitor is required. The input capacitor should be located as close as possible to the IC. PGND is connected to the ground terminal of the input cap which then connects to the ground plane. The P_{VIN} is connected to the V_{BAT} terminal of the input capacitor which then connects to the V_{BAT} plane.

Layout and PCB Design Recommendations

Good PCB layout helps high power dissipation from a small package with reduced temperature rise. Thermal layout guidelines are:

- A four or more layers PCB board with solid ground planes is preferred for better heat dissipation.
- More free vias are welcome to be around IC to connect the inner ground layers to reduce thermal impedance.
- Use large area copper especially in top layer to help thermal conduction and radiation.
- Use two layers for the high current paths (P_{VIN}, PGND, SW, V_{OUT}) in order to split current in two different paths and limit PCB copper self heating.

(See demo board example Figure 39)

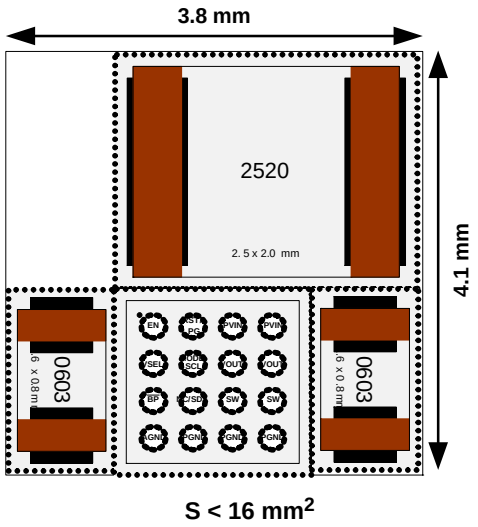


Figure 39. Layout Minimum Recommended Occupied Space

Input capacitor placed as close as possible to the IC.

P_{VIN} directly connected to C_{IN} input capacitor, and then connected to the P_{VIN} plane. Local mini planes used on the top layer (green) and layer just below top layer with laser vias.

PGND directly connected to C_{IN} input capacitor, and then connected to the GND plane: Local mini planes used on the top layer (green) and layer just below top layer with laser vias.

SW connected to the LX inductor with local mini planes used on the top layer (green) and layer just below top layer with laser vias.

V_{OUT} directly connected to C_{OUT} output capacitor and then connected to PGND plane

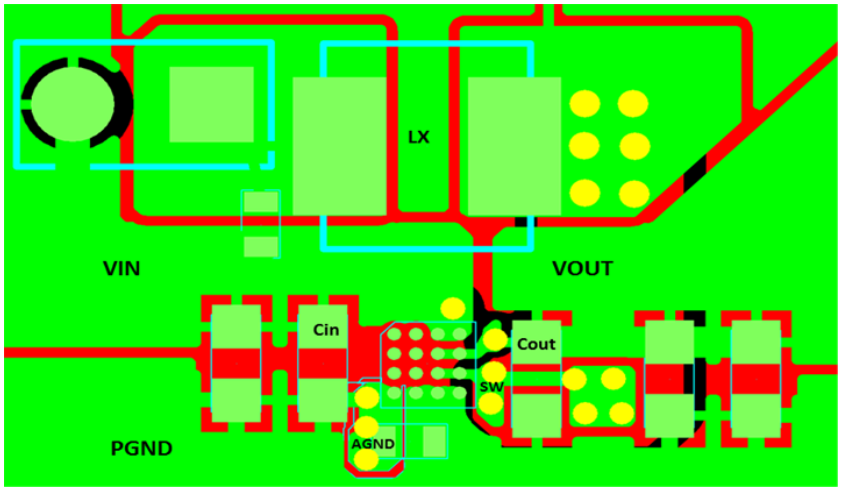


Figure 40. Example of PCB Implementation

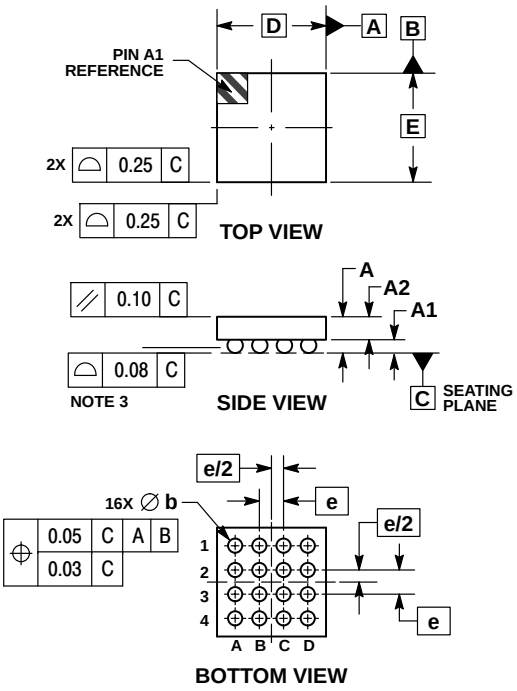
Table 24. ORDERING INFORMATION

Device*	Package	Shipping†
NCP6868PFCCT1G	WLCSP16 (Pb-Free)	3000 / Tape & Reel
NCP6868V300FCCT1G	WLCSP16 (Pb-Free)	3000 / Tape & Reel
NCP6868V315FCCT1G	WLCSP16 (Pb-Free)	3000 / Tape & Reel
NCP6868V330FCCT1G	WLCSP16 (Pb-Free)	3000 / Tape & Reel
NCP6868V350FCCT1G	WLCSP16 (Pb-Free)	3000 / Tape & Reel
NCP6868V360FCCT1G	WLCSP16 (Pb-Free)	3000 / Tape & Reel
NCP6868V370FCCT1G	WLCSP16 (Pb-Free)	3000 / Tape & Reel
NCP6868V450FCCT1G	WLCSP16 (Pb-Free)	3000 / Tape & Reel
NCP6868V500FCCT1G	WLCSP16 (Pb-Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
*Consult Sales Office for specific Output Voltage requirement

PACKAGE DIMENSIONS

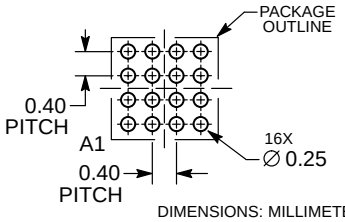
WLCSP16 1.80x1.80
CASE 567JU
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. COPLANARITY APPLIES TO SPHERICAL CROWNS OF SOLDER BALLS.

	MILLIMETERS	
DIM	MIN	MAX
A	−−−	0.60
A1	0.17	0.23
A2	0.36 REF	
b	0.24	0.29
D	1.80 BSC	
E	1.80 BSC	
e	0.40 BSC	

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800−282−9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
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Phone: 81−3−5817−1050

ON Semiconductor Website: **www.onsemi.com**

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative

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